Design of High Gain, Two-Stage CMOS Operational Amplifier

Shruti, B.E Electronics and Instrumentation, Birla Institute of Technology and Science, Pilani
Deeksha Dadhich, B.E Electronics and Instrumentation, Birla Institute of Technology and Science Pilani
Meher Gitika, B.E Electronics and Instrumentation, Birla Institute of Technology and Science, Pilani

ABSTRACT

This paper presents a design of two stage single ended CMOS operational amplifier, which operates at ±3.3V power supply using tsmc 180nm CMOS technology. The OPAMP designed has two-stages and a single ended output and is designed to exhibit a unity gain frequency of 100MHz, gain of 83.52dB with a 60 degree phase margin to work with a load capacitance of 500fF and have power dissipation less than 3mW. Design and Simulation has been carried out in Cadence.

Keywords
180nm CMOS technology, Two Stage single ended CMOS operational amplifier

1. INTRODUCTION

The continuous trend of scaling down transistor size allows the integration of more number of transistors on the same size of chip hence reducing time delays. This results in continuous increase in the processing capacity and operating frequency. Operational Amplifiers is one of the most commonly used building blocks of electronic circuits. Opamp based circuits are more precise, insensitive to noise and are less susceptible to fluctuations. Design of a stable operational amplifier with a high gain and high unity gain bandwidth with continuously reducing power supply and channel length is a major challenge. There is always a trade off among various parameters such as bandwidth, speed, gain, power dissipation. With higher gain and bandwidth the speed and accuracy of the amplifier increases but the stability in negative feedback decreases.

Aim is to build an opamp with a fairly high gain and unity gain bandwidth at a maximum phase margin to ensure stability. Various compensation techniques can be adopted to achieve this.

2. TWO STAGE AMPLIFIER TOPOLOGY

2 stage operational amplifiers consist of a differential amplifier in the 1st stage followed by a Common Source Amplifier in the 2nd stage. Differential Amplifier stage is to ensure high gain and CSA stage is to further increase the gain an also provide high voltage swing at the output. The block diagram of a two stage operational amplifier is shown in Fig.1.

![Fig.1 Two Stage Amplifier](image)

The 1st block is a differential amplifier. It has two inputs, an inverting input and non inverting input. It can give a differential voltage or single ended voltage, depending on the configuration at the output which depends on differential input voltage. Single ended output degrades the output swing of the amplifier. Also the Common Mode Rejection Ratio degrades as the symmetry of the circuit is lost.

In circuits where the gain provided by the differential amplifier stage is not enough, additional amplification required is provided by the second stage, i.e. the common source amplifier, driven by the output of the first stage. The biasing circuit provides the proper operating point to each transistor in its saturation region. An output buffer stage can be attached at the end to provide the low output impedance and larger output current needed to drive the load. For a small capacitive load output buffer is not required. When the output buffer stage is not used, the circuit acts as an operational transconductance amplifier or OTA.

3. CIRCUIT IMPLEMENTATION

The circuit comprises of three subparts: the differential gain stage, second gain stage and biasing circuit. MOSFETS M1, M2, M3, M4, M5 form the differential amplifier stage. M6 and M7 form the second gain stage and are in Common Source Amplifier Configuration. M8 and the Current source form the biasing circuitry.
Fig.2 Two stage amplifier topology

3.A Differential Gain Stage:
It is made up of MOSFETS M1, M2, M3, M4 and M5 as shown in Fig.2. Positive input is given to the gate of M1 and negative input is given to the gate of M2. M3 and M4 from the PMOS current mirror load of this stage. The gain of this stage is given by:

\[ \text{GAIN}_1 = g_{m2} + g_{mb2}(r_{o1} || r_{o4}) \]
\[ = [g_{m2} + g_{mb2}]r_{o2}r_{o3} / (r_{o2} + r_{o4}) \]

Where, \( g_{m2} \) = transconductance of M2
\( g_{mb2} \) = backgate transconductance of M2

The current mirror load provides for conversion of differential input to single ended output and also provides higher gain as compared to passive loads. The differential current from M1 and M2 multiplied by the output resistances of the input stage gives the single-ended output voltage, which is fed as input to the next stage.

3.B Common Source Amplifier Stage:
The second stage is a common source topology amplifier. The purpose of the second stage is to provide additional gain and a high output swing. It is made up of transistors M6 and M7. The output from the drain of M2 is fed as input to the gate of M6. The MOSFET M7 serves as load to the driver MOSFET M6. The gain of this stage is given by:

\[ \text{GAIN}_2 = (g_{m6} + g_{mb6})(r_{o6} || r_{o7}) \]
\[ = [(g_{m6} + g_{mb6})r_{o6}r_{o7}] / (r_{o6} + r_{o7}) \]

Where, \( g_{m6} \) = transconductance of M6
\( g_{mb6} \) = backgate transconductance of M6

Therefore, total gain at the output of the opamp is:

\[ \text{GAIN} = \text{GAIN}_1 \ast \text{GAIN}_2 \]
\[ = (g_{m2} + g_{mb2})[(g_{m6} + g_{mb6})(r_{o6} || r_{o7})(r_{o2} || r_{o4}) \]

3.C Biasing Circuitry:
Current source, I_s in fig.2 acts as a reference source for transistor M8. I_s and M8 form a current mirror biasing network driving the transistors, M5 and M7 which act as current sinks. The gate to source voltage of M5 and M7 is controlled by this bias network.

3.D RC Compensation:
\( R_c \) and \( C_c \) are used between gate and drain of M6 to improve the phase margin and hence stability of the circuit.

4. DESIGN OF THE CIRCUIT
The circuit was designed to meet the following specifications as in Table.1.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power supply</td>
<td>3.3 V</td>
</tr>
<tr>
<td>Gain</td>
<td>Greater than 15000/vv</td>
</tr>
<tr>
<td>Unity Gain Bandwidth</td>
<td>Greater than 100 MHz</td>
</tr>
<tr>
<td>Phase Margin</td>
<td>Greater than 60°</td>
</tr>
<tr>
<td>Load Capacitance</td>
<td>Greater than 500F</td>
</tr>
<tr>
<td>Power Dissipation</td>
<td>Less than 3mW</td>
</tr>
</tbody>
</table>

To validate the theoretical results, we first implemented the two stage operational amplifier through approximate models with the specifications mentioned in Table.2.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Channel length</td>
<td>500nm</td>
</tr>
<tr>
<td>Load capacitance</td>
<td>1pF</td>
</tr>
<tr>
<td>( \mu ) C_{ox}</td>
<td>150\mu</td>
</tr>
<tr>
<td>( \mu F ) C_{ox}</td>
<td>60 \mu</td>
</tr>
<tr>
<td>Unity Gain Bandwidth</td>
<td>110MHz</td>
</tr>
<tr>
<td>Phase margin</td>
<td>60°</td>
</tr>
<tr>
<td>Slew rate</td>
<td>43.18V/\mu s</td>
</tr>
<tr>
<td>Threshold voltage of all MOSFETS</td>
<td>0.7V</td>
</tr>
</tbody>
</table>

Other parameters are calculated with the help of the parameters mentioned in Table.2.

4.A Calculating \( C_c \)
For 60 degree phase margin-
\( C_c \geq 0.22 \ast C_l \)
\( C_c = 0.22pF \)

4.B Calculating \( g_{m1} \) and \( g_{m6} \)
\( UGB = g_{m1}/2\pi C_c \) and \( UGB = 110MHz \)
Also, \( g_{m6} \geq 10 \ast g_{m1} \)
We obtain, \( g_{m1} = 145\mu \) and \( g_{m6} = 1450\mu \)

4.C Calculating \( I_s, I_1, I_2, (W/L)_1, (W/L)_2, g_{m4} \)
Slew Rate ≥ \( I_1 /C_c \) (assuming Slew Rate = 43.18V/\mu s)
\[ I_s = 9.5\mu A \]
\[
I_1 = I_2 = 4.75 \mu A
\]
\[
I_3 = I_4 = 4.75 \mu A
\]

We know,
\[
I_d = 0.5 \mu C_{ox} (W/L) (V_{ov})^2
\]
\[
(W/L)_1 = \frac{g_{m3}}{\mu C_{ox}} (W/L)_2 (2I_2)
\]
\[
(W/L)_1 = (W/L)_2 = 15
\]

4. D Calculating \((W/L)_3\), \((W/L)_4\), \((W/L)_5\), \((W/L)_6\), \((W/L)_7\), and ICMR

As overdrive voltages of PMOS are greater than those of NMOS, we have assumed it to be 1.5 times larger than that of NMOS
\[
V_{ov, M6} = V_{ov, M3} = V_{ov, M4} = 0.3V
\]
\[
V_{ov, M7} = V_{ov, M1} = V_{ov, M2} = 0.2V
\]
\[
V_{ov, M5} = V_{ov, M8} = 0.3V
\]

Using the saturation drain current equation we get
\[
(W/L)_3 = (W/L)_4 = 2
\]
\[
(W/L)_5 = (W/L)_6 = \frac{I_6}{I_4}
\]
\[
(W/L)_6 = \frac{2 \mu C_{ox} (W/L)_6 I_6}{0.5} = 35 \mu A
\]
\[
(W/L)_6 = 82.85
\]
\[
(W/L)_7 = (W/L)_8 = I_7/I_4
\]
\[
I_6 = I_7 = 196.768 \mu A
\]
\[
I_{CMR+} = V_{DD} - V_{gs, M3} + V_{th, M1} = 3V
\]
\[
I_{CMR-} = V_{ov, M1} + V_{th, M1} + V_{ov, M5} = 1.2V
\]

4. E FINAL PARAMETERS OF THE CIRCUIT :

MOSFETS M1, M2, M7 were operating under linear region when above aspect ratios were used. So, the current source supply was increased to 15µA. The values of W/L ratios for M1, M2, M6 and M7 were iterated to get all the MOSFETS to operate in saturation region. The final value of biasing current \(I_1 = 15 \mu A\). The final W/L ratios after iteration are listed in Table.3

<table>
<thead>
<tr>
<th>MOSFET</th>
<th>W/L RATIO</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1</td>
<td>4</td>
</tr>
<tr>
<td>M2</td>
<td>4</td>
</tr>
<tr>
<td>M3</td>
<td>2</td>
</tr>
<tr>
<td>M4</td>
<td>2</td>
</tr>
<tr>
<td>M5</td>
<td>1</td>
</tr>
<tr>
<td>M6</td>
<td>50</td>
</tr>
<tr>
<td>M7</td>
<td>12.2</td>
</tr>
<tr>
<td>M8</td>
<td>1</td>
</tr>
</tbody>
</table>

4. F RC Compensation

AC analysis of the above obtained circuit showed good gain and UGB sufficiently greater than the specifications but phase margin was very less (~10 degrees). So method of RC compensation was followed to increase the phase margin.

The final values of \(C_C, R_C\) and \(C_L\) used were:
\[
C_C = 145F
\]
\[
R_C = 3K\Omega \text{ (for compensation)}
\]
\[
C_L = 500F
\]
\[
R_L = 1K\Omega
\]

5. SIMULATION AND RESULTS

All the simulations were done on Cadence Virtuozo with 180 nm technology using a \(V_{DD}\) of 3.3V. The load capacitance was taken to be 1pF for all the simulations.

![Fig.3 Snapshot from Virtuozo of Proposed Design Schematic](image)

The procedure for the simulations is - first of all DC analysis was done to ensure saturation for all transistors. After that, the AC analysis with differential input signal as 1V peak to peak was given to measure the gain, GBW, UGB and Phase margin. After the AC analysis, a transient analysis was done to measure the slew rate and settling time (1%). For the transient analysis, the input signal was given as a square pulse of amplitude 1V at 5MHz.

The results obtained after simulation are tabulated in Table.4

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>VALUES OBTAINED</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gain</td>
<td>22310.022 V/V</td>
</tr>
<tr>
<td>UGB</td>
<td>103.8 MHz</td>
</tr>
<tr>
<td>Phase margin</td>
<td>61.39º</td>
</tr>
<tr>
<td>Power Dissipation</td>
<td>712µW</td>
</tr>
<tr>
<td>Slew rate</td>
<td>87.16V/µs</td>
</tr>
</tbody>
</table>

After this, the stability analysis was carried out to check the operation of the amplifier in closed loop configuration with varying input differential voltages and the output voltage was recorded as shown in the Figure 4.
By AC-Analysis we determine Phase margin, Gain and Unity Gain Bandwidth of the Opamp.

Figure 5 shows the gain, UGB and the phase margin obtained with STB Analysis.

Gain: 86.97dB = 22310.022 V/V
UGB: 103.8 MHz
Phase Margin: 61.39°

Transient Analysis helps to determine the slew rate and settling time of op-amp.

Figure 6 shows the transient response carried through the STB analysis.
Slew rate from the figure 6 is obtained as:  
Slew rate = Slope of linear portion = 0.6877V/(31.93-24.04)ns
         = 87.16V/us

The DC response of the analysis was carried out and ICMR was plotted as shown in the figure 8.

6. CONCLUSION

This paper presented the full custom design of a two stage CMOS Op-Amp and analyzed its behaviour for various aspect ratios. Design technique for this Op-Amp, its calculations and computer-aided simulation results are given in detail. In the Design of a two-stage op-amp optimization of one or more parameters can lead to degradation of others. The increase in the Unity Gain Bandwidth has been done by increasing the bias current. This decreases the gain and increases power dissipation slightly, but it provides a good alternative control to increase bandwidth. Introduction of each stage adds an additional pole which can lead to instability. Hence a proper compensation technique has been employed in the system. For this reason the RC-Miller compensation technique has been employed. The results show that the designed amplifier has successfully satisfied all the specifications given. Tables and graphs of different parameters for various aspect ratios are drawn. Similar analysis has also been carried out in different corners (ss, ff and tt) and temperatures where it was found that all the specifications mentioned have been satisfied.
7. REFERENCES